IN THE CLAIMS

Please amend the claims as follows:

Claim 27 (New): Sealing processing for two wafers made of semiconducting materials, comprising:

- a step for implantation of metallic species in at least the first wafer,
- a step for assembly of the first and second wafer by molecular bonding,
- a step for formation of metallic compounds, alloys between the implanted metallic species and the semiconducting materials of the two wafers, said metallic compound forming a resistive contact between the two wafers, at the assembly interface.

Claim 28 (New): Process according to claim 27, the formation step of the metallic compounds resulting from a heat treatment at a temperature equal at least to the formation temperature of the said compounds.

Claim 29 (New): Process according to claim 27, the metallic species being implanted at a depth (Rp) of between 5 nm and 20 nm under the surface of the implanted wafer.

Claim 30 (New): Process according to claim 27, the metallic species being implanted at a dose of between 10^{14} and a few 10^{18} species/cm^2.

Claim 31 (New): Process according to claim 27, also comprising an amorphisation step before assembly to make all or part of the surface layer of the first wafer amorphous.

Claim 32 (New): Process according to claim 31, the amorphisation step comprising deposition of an amorphous material layer before and/or after implantation of metallic species.

Claim 33 (New): Process according to claim 31, the amorphisation step comprising a surface implantation, for example by hydrogen or metallic species.

Claim 34 (New): Process according to claim 27, each of the wafers being made from a material chosen from among silicon, gallium arsenide (GaAs), SiC (silicon carbide), InP (Indium phosphide), Germanium (Ge), le silicon - Germanium (SiGe).

Claim 35 (New): Process according to claim 27, the implanted species being Nickel and/or palladium and/or Cobalt, and/or Platinum, and/or Tantalum, and/or Tungsten, and/or Titanium, and/or Copper.

Claim 36 (New): Process according to claim 27, at least one of the wafers being a heterostructure, for example of the SOI type.

Claim 37 (New): Process according to claim 27, at least one of the wafers being thinned, after assembly or after the formation step of metallic compounds.

Claim 38 (New): Process according to claim 27, at least one of the wafers being a debondable structure.

Claim 39 (New): Process according to claim 27, at least one of the wafers comprising a weakening plane.

Claim 40 (New): Process according to claim 27, the wafer comprising a weakening plane being thinned by fracture along the said weakening plane, after assembly or after the formation step of the metallic compounds.

Claim 41 (New): Process according to claim 27, at least one of the wafers comprising at least one circuit or circuits layer, on or close to its face to be assembled.

Claim 42 (New): Process according to claim 27, the implantation step of metallic species being done through a mask to obtain local implantation zones.

Claim 43 (New): Process according to claim 27, also comprising the formation of an insulating layer on the first wafer, before it is implanted with metallic species.

Claim 44 (New): Process according to claim 27, also comprising a thinning step of the implanted wafer after implantation of metallic species.

Claim 45 (New): Process according to claim 27, the first wafer comprising at least one insulating zone located at the surface so as to obtain local implantation zones.

Claim 46 (New): Structure comprising two substrates made of semiconducting materials assembled by molecular bonding and having localised zones of metallic compounds at the assembly interface, these metallic compounds being alloys made from semiconducting

materials of substrates at the assembly interface and at least one metal chosen from among nickel, palladium, cobalt, platinum, tantalum, tungsten, titanium, copper.

Claim 47 (New): Structure according to claim 46, the semiconducting materials being chosen from among Si, GaAs, SiC, InP, SiGe.

Claim 48 (New): Structure according to claim 46, at least one of the substrates being a heterostructure.

Claim 49 (New): Structure according to claim 46, at least one of the substrates being a thin film.

Claim 50 (New): Structure according to claim 46, at least one of the substrates comprising electronic and/or optical and/or mechanical components.

Claim 51 (New): Structure according to claim 46, one of the substrates being a thin film made of silicon comprising RF circuits.

Claim 52 (New): Structure according to claim 51, the other substrate being made of high resistivity silicon.

Claim 53 (New): Sealing processing for two wafers made of semiconducting materials, comprising:

- a step for implantation of metallic species in at least the first wafer, at a depth (Rp) of between 5 nm and 20 nm under the surface of said first wafer, at a dose of between 10^{14} and a few 10^{18} species/cm^2,

- a step for assembly of the first and second wafer by molecular bonding,

- a step for formation of metallic compounds, alloys between the implanted metallic species and the semiconducting materials of the two wafers, said metallic compound forming a resistive contact between the two wafers, at the assembly interface.

Claim 54 (New): Process according to claim 53, the formation step of the metallic compounds resulting from a heat treatment at a temperature equal at least to the formation temperature of the said compounds.

Claim 55 (New): Process according to claim 53, also comprising an amorphisation step before assembly to make all or part of the surface layer of the first wafer amorphous.

Claim 56 (New): Process according to claim 55, the amorphisation step comprising deposition of an amorphous material layer before and/or after implantation of metallic species.

Claim 57 (New): Process according to claim 55, the amorphisation step comprising a surface implantation, for example by hydrogen or metallic species.

Claim 58 (New): Structure obtained by a process according to claim 27, comprising two substrates made of semiconducting materials assembled by molecular bonding and having localised zones of metallic compounds at the assembly interface, these metallic

compounds being alloys made from semiconducting materials of substrates at the assembly interface and at least one metal chosen from among nickel, palladium, cobalt, platinum, tantalum, titanium, copper.

Claim 59 (New): Structure according to claim 58, the semiconducting materials being chosen from among Si, GaAs, SiC, InP, SiGe.

Claim 60 (New): Structure according to claim 58, at least one of the substrates being a heterostructure.

Claim 61 (New): Structure according to claim 58, at least one of the substrates being a thin film.

Claim 62 (New): Structure according to claim 58, at least one of the substrates comprising electronic and/or optical and/or mechanical components.

Claim 63 (New): Structure according to claim 58, one of the substrates being a thin film made of silicon comprising RF circuits.

Claim 64 (New): Structure according to claim 63, the other substrate being made of high resistivity silicon.